Off-State Leakage Induced by Band-to-Band Tunneling and Floating-Body Bipolar Effect in InGaAs Quantum-Well MOSFETs

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***Abstract*— The physics of off-state drain leakage (I_{off}) in scaled self-aligned InGaAs quantum-well (QW) MOSFETs is investigated through experiments and simulations. Excess I_{off} is observed in InGaAs QW-MOSFETs with very short contact-to-channel spacing. This current bears the marks of band-to-band tunneling (BTBT) that takes place at the drain edge of the channel. However, a pure BTBT current does not explain the observed magnitude of I_{off} nor its gate length dependence. For this, we invoke floating-body bipolar amplification of the BTBT current in the QW channel. Device simulations that include BTBT and drift diffusion are consistent with the magnitude of the experimental I_{off} and its gate length scaling behavior. The understanding derived here suggests a number of paths to mitigate BTBT-induced off-state current in scaled InGaAs QW-MOSFETs.**

***Index Terms*— III-V, floating body, bipolar effect, BTBT, self-aligned, quantum-well MOSFETs.**

I. Introduction

InAs-RICH InGaAs is a promising channel material for future CMOS applications due to its superior electron transport properties [1]–[5]. Enhancing the InAs composition of InGaAs increases the electron mobility and injection velocity but reduces the bandgap. This is problematic because it can bring about excessive leakage current that prevents the effective turning-off of the transistor. In fact, in high-transconductance InGaAs MOSFETs with tight source/drain (S/D) to gate distance, excessive off-state current with a characteristic Gate-Induced Drain Leakage (GIDL, [6], [7]) signature has been reported [2], [3]. GIDL takes place in the high electric field region at the drain-end of the channel and is a manifestation of a band-to-band tunneling process (BTBT). To address this issue, designs using a more relaxed access region [2] or including an undoped spacer [3] have been shown to reduce the high E-field and suppress I_{off}. In spite of this, at the moment, there is a lack of detailed physical understanding of the relevant mechanisms at play. In particular, no consideration has been given to the quantum-well nature of the channel and the potential for a floating-body effect mechanism that can amplify the GIDL current. In floating-body Silicon-on-Insulator (SOI) MOSFETs, it is well-known that the presence of a lateral bipolar junction transistor (BJT) with substantial current gain yields a dramatic enhancement of BTBT or impact-ionization generated current [8]–[11]. The current gain of the lateral BJT depends strongly on channel length. In this work, we show that a phenomenon of this nature takes place in quantum-well InGaAs MOSFETs and that this is responsible for the large off-state current that we experimentally observe. This work extends the experimental study of [2].

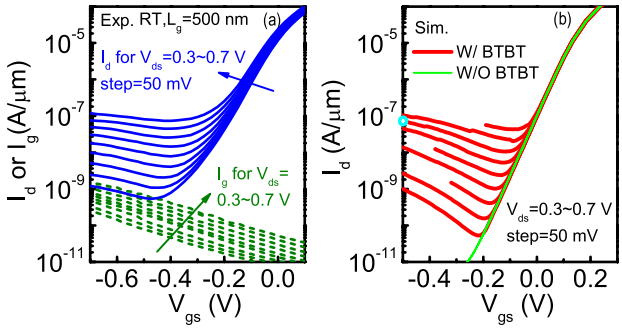

Fig. 1. (a) Experimental room temperature (RT) subthreshold and gate current characteristics of long-channel InGaAs MOSFETs. (b) Simulated subthreshold characteristics with and without BTBT model suggesting that BTBT plays a role in the excess off-state current.

II. Self-Aligned InGaAs QW-MOSFETs

The devices in this study are fabricated by a tight-pitch process as reported in [2]. These are self-aligned QW-MOSFETs with 8-nm thick composite channel consisting of an InAs core (2 nm) and two $In_{0.7}Ga_{0.3}As$ cladding layers.

Our self-aligned fabrication process is based on precision RIE and digital etch. It allows us to create a highly-conducting "ledge" that spans the access region right next to the gate with the goal of minimizing source and drain resistance while preserving a tight device pitch. In devices with very short ledge (∼5 nm), BTBT becomes significant at the drain edge when the drain is biased to V_{dd} and the gate is turned off [2]. Fig. 1(a) shows the subthreshold I_d–V_{gs} characteristics of a $L_g = 500$ nm device at room temperature. I_d flows directly from D to S, as I_g is significantly smaller than I_{off} over the entire voltage span for all devices that we have studied. In particular, for $V_{ds} > 0.5$ V, $|I_g/I_d|$ is less than 3%. We also verify that buffer leakage is much lower than I_{off}.

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Excess off-state drain current is noticeable. In [2] we showed that this excess off-state current bears the marks of BTBT, i.e., it exhibits a voltage dependence characteristic of BTBT and its temperature dependence follows that of the bandgap of the channel. Following the Si MOSFET notation, we are in front of a GIDL current [6], [7].

To understand the BTBT process and the off-state current in these devices, we build a 2D TCAD device model in Synopsys Sentaurus Device [12]. In these simulations, coupled Poisson, electron and hole continuity equations are solved self-consistently with and without a non-local path BTBT model. The device structure closely follows [2] except that in the extrinsic source and drain region, the 3-nm InP etch-stop is substituted by $In_{0.53}Ga_{0.47}As$ for improved numerical convergence. Recombination is assumed to take place only at the S/D metal contacts which are characterized by an infinite surface recombination velocity. The contacts are long enough for their length not to be relevant. Recombination in the body of the channel and the cap is neglected as the diffusion length for holes is estimated to be much longer than the gate length and the cap thickness. This estimation is based on the experimental carrier lifetimes of an $In_{0.53}Ga_{0.47}As/InP$ structure [13]. We selected E_g for the $In_xGa_{1-x}As$ channel following Vegard's law based on the bulk values of InAs (0.35 eV) and GaAs (1.42 eV). The parameters that characterize the BTBT process were adjusted to provide order of magnitude agreement with the experimental results. For the purpose of obtaining high-level physical understanding, this was deemed adequate.

Results from our simulations are shown in Fig. 1(b). The rising tail of I_d with decreasing V_{gs} is observed only when the BTBT model is included; otherwise I_d continues to decrease with V_{gs} following the classic subthreshold behavior. In the simulations that include BTBT, the minimum current level in the off-state is close to the experimentally observed values. This strongly suggests that BTBT plays a role in the excess off-state current. Both subthreshold swing and the slope of drain leakage are steeper in the simulations. This is very likely the result of interface states that are not included in the simulations, but are active in RT measurements [2]. Interface states affect the slope of the drain current in the off regime as the gate control over the surface potential is degraded. No attempt was made to match measured and simulated V_t because we assume that work function tuning of the gate metal would readily induce the necessary parallel shift along the V_{gs} axis.

A pure BTBT nature of the off-state current would imply an absence of gate length dependence. That is not what is experimentally observed. Fig. 2(a) shows experimental $I_d - V_{gs}$ characteristics of transistors with L_g from 80 nm to 500 nm at 200 K and at $V_{ds} = 0.7$ V. For clarity, the voltage axis is shifted by the V_t of the respective transistor. We use low temperature data to freeze-out the interface states and reduce their influence on the subthreshold behavior of the transistor [2]. I_{off} is observed to increase as L_g is reduced. Fig. 2(b) plots the inverse of I_d *vs.* L_g for $V_{ds} = 0.7$ V and three $V_{gs} - V_t$ values. The strong inverse dependence of off-state I_d with L_g cannot be explained by a pure BTBT-induced current.

In order to understand the L_g dependence of the off-state current, Fig. 3 (a) shows simulated contours of BTBT generation rate, G, at the edge of the gate near the drain

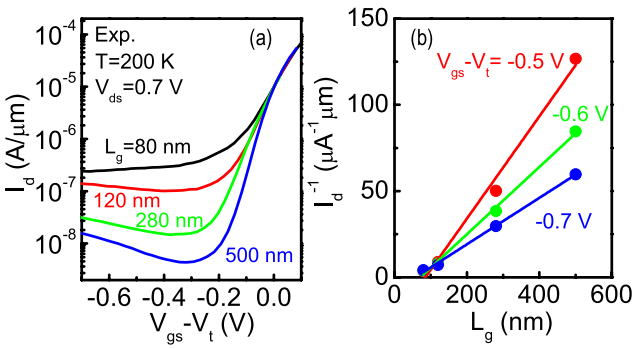

Fig. 2. (a) Experimental subthreshold characteristics of InGaAs MOSFETs for gate lengths between 80 and 500 nm, measured at $V_{ds} = 0.7$ V and at 200 K. (b) I_d^{-1} *vs.* L_g at fixed V_{ds} and V_{gs}–V_t under the same measurement conditions of (a).

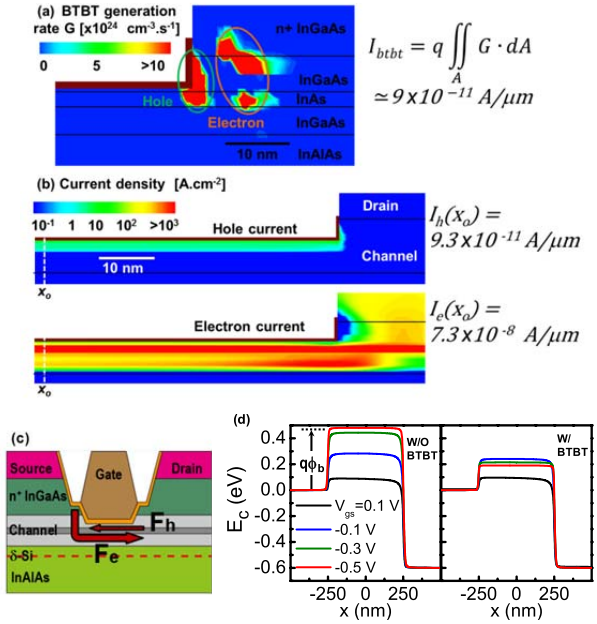

Fig. 3. (a) BTBT coutours for electrons (right circle) and holes (left circle) at the drain edge of the channel. The channel consists of $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As = 1/2/5$ nm [2]. Electron generation takes place in two regions: around the n^+/undoped InGaAs junction as a result of the strong band bending and in the InAs core because of its narrow bandgap. (b) Electron and hole current density corresponding to the same situation as in (a). The currents per unit gate width at point x_o are indicated on the right. (c) Device structure schematic illustrating electron and hole fluxes in the channel in the off-state in the presence of BTBT. (d) Conduction band-edge diagram along the middle of the InAs channel core from source to drain with and without BTBT model.

contact for a $L_g = 500$ nm device at $V_{ds} = 0.6$ V and $V_{gs} = -0.5$ V. The selected bias corresponds to the point labeled with an "O" mark on the y-axis in Fig. 1 (b). Since the maximum E-field occurs at the top surface of the channel near the drain edge, BTBT takes place around this high-field region: electron generation prevails in the circled right side area of Fig. 3(a) while hole generation mainly occurs in the channel surface near the gate edge (left circled area). The BTBT generation rate depends strongly on the E-field, or, in essence, V_{gd}. It exhibits negligible dependence on gate length. The magnitude of the BTBT current per unit width, I_{btbt}, can be calculated by integrating the generation rate

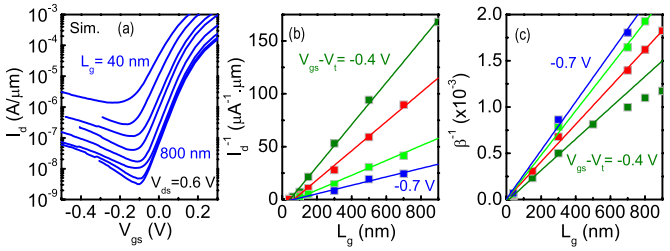

Fig. 4. (a) Simulated subthreshold characteristics for various L_g. (b) I_d^{-1} *vs.* L_g and (c) β^{-1} *vs.* L_g at $V_{ds} = 0.6$ V and various $V_{gs} - V_t$.

of either electrons or holes. Here we use hole generation (left circle) to estimate the BTBT current as shown in Fig. 3 (a). It is approximately 9×10^{-11} A/μm, about three orders of magnitude smaller than I_d calculated at this bias point (in Fig. 1b) or observed experimentally (Fig. 1a).

To understand this discrepancy, we further explore the simulated current components by plotting the electron and hole current magnitude contours in the channel. These are shown in Fig. 3(b). Generated holes flow towards the source on the left, while electrons flow towards the drain on the right. Along the x-direction under the gate, both carrier currents are largely location independent. It is observed that the electron current is much higher than the hole current. We define the total electron (hole) current per unit width, $I_e(I_h)$, as the integration of the electron (hole) current magnitude along the y-axis. At x = x_o in Fig. 3(b) we obtain I_h of 9.3×10^{-11} A/μm, matching the BTBT current in Fig. 3(a). Meanwhile, I_e of 7.3×10^{-8} A/μm matches the I_d calculated at this bias (label "O" in Fig. 1b). There is then a current gain in this situation of $\beta = I_e/I_h = 780$.

The study of Fig. 3 is carried out on a long gate length device ($L_g = 500$ nm). When L_g scales down, the gain becomes much higher and I_{off} increases. This is clear in the simulated subthreshold characteristics of transistors of different L_g at $V_{ds} = 0.6$ V shown in Fig. 4(a). The drain current also becomes more independent of V_{gs} at shorter L_g, consistent with Fig. 2(a). The underlying reason is that the source-channel barrier ($q\phi_b$) height is nearly pinned *vs.* V_{gs} in the presence of hole generation by BTBT. The modulation of $q\phi_b$ is clearly seen in the conduction band-edge diagrams through the middle of the InAs core along the channel from source to drain with and without the BTBT model, as shown in Fig. 3(d). Fig. 4(b) plots $I_d^{-1} vs \cdot L_g$ for different values of V_{gs} for the same V_{ds} of 0.6 V. From the simulations we also extract β. Fig. 4(c) graphs $\beta^{-1} vs \cdot L_g$. For a given value of $V_{gs} - V_t$, I_d^{-1} and β^{-1} increase almost linearly with L_g, a typical bipolar effect signature. Fig. 4(b) also shows that for a given L_g, I_d increases as $V_{gs} - V_t$ becomes more negative. This is consistent with the experimental data in Fig. 2.

The physics that are at play here are then clear. In essence, as illustrated in Fig. 3(c), BTBT generated holes are collected in the quantum well. Since there is no well contact, the holes pile up. This results in a reduction of the barrier that holes need to be overcome to be injected into the source where they recombine. The reduction of the barrier leads to electron injection from the source into the channel. This is the excess off-state current that we observe. The current gain as seen in Fig. 4(c) is large (>500) but not uncommon. In Si MOSFETs, bipolar gains of a few thousand have been reported for L_g of 250 nm [14], [15]. Shorter devices exhibit higher current gain. Also, more negative $V_{gs} - V_t$ increases the barrier and yields a lower value of beta (Fig. 4c). In spite of this, I_d continues to increase as $V_{gs} - V_t$ becomes more negative. This is because BTBT generation becomes more prominent.

In order to minimize off-state leakage in InGaAs MOSFETs, it is imperative to address both BTBT and the bipolar gain effect. One path that has been implemented in SOI MOSFETs consists of enhancing the recombination process before the generated minority carriers reach the source [16]. III-V heterostructure design also provides freedom to engineer the bandgaps of the n^+ S/D and channel to mitigate BTBT and the bipolar gain. Besides, the geometrical design of the channel, source and drain play a significant role in the bipolar gain effect. Further studies are required.

III. Conclusion

The origin of high off-state leakage in quantum-well InGaAs MOSFETs has been investigated. This current bears the characteristic signature of BTBT but scales inversely with gate length suggesting an additional bipolar gain mechanism as in SOI MOSFETs. 2D simulations support this notion.

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